What is claimed is:

1. A method of forming a memory comprising:

forming an activation device for a memory cell, the activation device having a gate; and

forming the gate for the activation device as a gate segment that is separated by and self-aligned with a shallow trench isolation region, wherein forming the gate segments for the activation device includes depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and drain.

2. The method of claim 1, wherein the method further includes coupling a sub-lithographic word line to the gate of the activation device.

3. The method of claim 1, wherein the method further includes forming a stacked capacitor coupled to the activation device for storing data for the memory cell.

4. A method of forming a memory comprising: √

forming an array of memory cells interconnected with a plurality of bit lines and word lines, wherein forming each cell includes forming an activation device with gates formed as gate segments that are separated by and self-aligned with a shallow trench isolation region; and

coupling an addressing circuit to the array of memory cells to allow selective access to the memory cells, wherein forming the gate segments for the activation device includes depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and drain.

5. The method of claim 4, wherein forming an array of memory cells includes forming a plurality of cells in a folded bit line configuration.

6. The method of claim 4, wherein forming an array of memory cells includes forming stacked capacitors for storing data.

7. A method of forming a memory comprising:

providing a processor; and

coupling a memory device to the processor, the memory device formed by a method including:

forming an array of memory cells interconnected with a plurality of bit lines and word lines, the word lines including sub-lithographic word lines, forming each cell includes forming an activation device with gates formed as gate segments that are separated by and self-aligned with a shallow trench isolation region; and

coupling an addressing circuit to the array of memory cells to allow selective access to the memory cells, wherein forming the gate segments for the activation device includes depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and drain.

8. The method of claim 7, wherein forming an array of memory cells includes forming a plurality of cells in a folded bit line configuration.

9. The method of claim 7, wherein forming an array of memory cells includes forming stacked capacitors for storing data.

10. The method of claim 7, wherein forming the memory device includes forming a dynamic random access memory.

11. The method of claim 7, wherein the method further includes forming the memory as a memory system with the processor provided external to the memory device.

12. A method of forming a memory comprising:

providing a control circuit; and

coupling a memory device to the control circuit, wherein the memory device is formed by a method including:

forming an array of memory cells interconnected with a plurality of bit lines and word lines, forming each cell includes forming an activation device with gates formed as gate segments that are separated by and self-aligned with a shallow trench isolation region;

coupling an addressing circuit to the array of memory cells to allow selective access to the memory cells, wherein forming each gate segment for the activation device includes:

forming a shallow trench isolation region with a pad that extends outwardly from a layer of a semiconductor material;

depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and a drain region associated with the gate being formed;

planarizing the conductive layer such that a working surface of the conductive layer is substantially coplanar with a surface of the shallow trench isolation region; and

selectively removing portions of the conductive layer and the insulating layer to provide a region for forming the gate segment.

13. The method of claim 12, wherein interconnecting a plurality of word lines with the array of memory cells includes selectively interconnecting sub-lithographic word lines with the gate segments.

14. The method of claim 12, wherein providing a control circuit includes providing a microprocessor.

15. The method of claim 12, wherein forming the memory device includes forming a dynamic random access memory.

16. The method of claim 12, wherein depositing a conductive layer includes depositing a poly-silicon layer.

17. The method of claim 12, wherein interconnecting a plurality of word lines with the array of memory cells includes forming the gate segments as a folded bit line array of memory cells.

18. The method of claim 12, wherein forming a shallow trench isolation region includes etching a trench into the layer of semiconductor material and filling the trench with an oxide layer, wherein the trench isolates a number of active regions.

19. The method of claim 12, wherein interconnecting a plurality of word lines with the array of memory cells includes selectively interconnecting a plurality of edge-defined word lines with the gate segments.

20. The method of claim 12, wherein the method further includes forming two gate segments in each active region defined by forming the shallow trench isolation region.

21. The method of claim 12, wherein the method further includes forming the memory as a memory system with the processor provided external to the memory device.

22. A method of forming a memory comprising

forming a pair of memory cells for an integrated circuit using a lithographic process having a minimum lithographic dimension, wherein forming the pair of memory cells includes:

forming two transistors in a semiconductor material, the transistors having a shared drain, each transistor having a gate and a source, the gate of each transistor formed as a gate segment that is separated by and self-aligned with a shallow trench isolation region, the gate of each transistor extending outwardly from the semiconductor material, wherein forming the gate segments for each transistor includes depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and drain;

forming two word lines outwardly from the transistors, wherein the word lines include sub-lithographic word lines with each word line having a width less than the minimum lithographic dimension, each word line connected to a gate of a different transistor, the word lines for activating the transistors;

forming a bit line and two conductors outwardly from the transistors, the bit line coupled to the shared drain of the transistors, each conductor coupled to the source of a different transistor, the bit line and the two conductors adjacent to the word lines; and

forming two storage capacitors outwardly from the bit line and the conductors, each storage capacitor coupled to a source of a different transistor by one of the conductors.

23. The method of claim 22, wherein the method further includes forming the memory as a dynamic random access memory.

24. The method of claim 22, wherein disposing a conductive layer includes depositing a poly-silicon layer.

25. The method of claim 22, wherein doping a source and drain for each transistor includes doping the source and drain for each transistor to provide a N+ source and a N+ drain.

26. A method of forming a memory comprising:

providing a microprocessor; and

coupling a memory device to the microprocessor, wherein the memory device is formed by a method comprising:

coupling a column decoder with input output circuitry to a plurality of bit lines and to a plurality of bit complement lines;

coupling a row decoder to a plurality of word lines;

coupling at least one address buffer to the row decoder and column decoder, wherein the address buffer receives an address of a selected cell and identifies a word line of the selected cell to the row decoder;

coupling each sense amplifier of a plurality of sense amplifiers to a corresponding pair of bit line and bit complement line; and

interconnecting an array of memory cells with the plurality of bit lines and word lines, the word lines including sub-lithographic word lines, wherein forming each cell includes forming an activation device with gates formed as gate segments that are separated by and self-aligned with a shallow trench isolation region, wherein forming the gate segments for the activation device includes depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and drain.

27. The method of claim 26, wherein interconnecting an array of memory cells includes interconnecting a plurality of cells formed in a folded bit line configuration.

28. The method of claim 26, wherein forming each cell includes forming a stacked capacitor for storing data.

29. The method of claim 26, wherein the method further includes forming the memory as an electronic system with the microprocessor provided external to the memory device.

30. A method of forming a memory comprising:

providing a controller; and

coupling a memory device to the controller, wherein the memory device is formed by a method comprising:

coupling a column decoder with input output circuitry to a plurality of bit lines and to a plurality of bit complement lines;

coupling a row decoder to a plurality of word lines;

coupling at least one address buffer to the row decoder and column decoder, wherein the address buffer receives an address of a selected cell and identifies a word line of the selected cell to the row decoder;

coupling each sense amplifier of a plurality of sense amplifiers to a corresponding pair of bit line and bit complement line; and

interconnecting an array of memory cells with the plurality of bit lines and word lines, wherein forming each cell includes forming an activation device with gates formed as gate segments that are separated by and self-aligned with a shallow trench isolation region, wherein forming the gate segments for the activation device includes depositing a conductive material and an insulating material after forming the shallow trench isolation region and before doping a source and drain.

31. The method of claim 30, wherein interconnecting an array of memory cells includes interconnecting a plurality of cells formed in a folded bit line configuration.

32. The method of claim 30, wherein forming each cell includes forming a stacked capacitor for storing data.

33. The method of claim 30, wherein providing a controller includes providing a microprocessor.

34. The method of claim 30, wherein the method further includes forming the memory as an electronic system with the controller provided external to the memory device.